A tunable CMOS transconductor for ultra-low Gm with wide differential input voltage range

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Abstract – **A differential input, single ended output transconductor with gm in the range 0.5-5 nS is presented. The circuit uses a source coupled pair operated in triode region. The need of providing a fixed common mode input voltage, which afflicts circuits based on the same principle, is removed by adopting an original topology. The results of simulations based on the 0.35 μm BCD6 process of STMicroelectronics are presented.**

1 INTRODUCTION

The research on low frequency fully integrated time continuous filters has recently received an important stimulus from the growing interest in micro-electro-mechanical systems and biomedical implantable apparatuses. For example, filtering the signal produced by pressure or flow sensors, in order to maximize the signal-to-noise ratio, requires singularities with frequencies of the order of a few Hz. The most popular approach to this problem is represented by Gm-C filters, thanks to their versatility and simple tuning techniques [1]. The low frequency involved in the applications mentioned above, together with the relatively small on-chip capacitance available in standard processes, requires G_m values of a few nS or below. In a CMOS transconductor, the voltage to current conversion is obtained applying the input and tuning signals to one or more transistors according to three possible combinations, shown in table 1 [1].

Method	Zone	Signal	Tuning
1	Saturation	V_{GS}	I_D
2	Triode	V_{DS}	V_{GS}
3	Triode	V_{GS}	V_{DS}

Table 1: Main methods to obtain a tunable Gm

In method 1 and 2, the G_m and the input differential range are both proportional to $\beta(V_{GS}-V_T)$, where, as customary, $\beta = \mu_n C_{ox} W/L$, W/L is the aspect ratio, μ_n is the electron mobility and C_{ox} the gate capacitance per unit area. Differently from the operational amplifier, a transconductor seldom works with virtual ground at its inputs, hence a large input range is generally required.

Therefore, methods 1 and 2 are not suitable to obtain a small G_m and, at the same time, a large input range. As it will be shown in the next section, method 3 gives the largest input range at the lowest end of the Gm tuning interval. Unfortunately the implementations of this method proposed so far, require that the input common mode voltage is constant [2,3]. This precludes application to single-ended architectures, which, while generally offering lower performances than fully differential ones, are much simpler to implement and less area consuming. In next sections a topology that does not suffer from this limitation is described and its effectiveness is tested by means of electrical simulations.

2 OPERATING PRINCIPLE

The core of the proposed transconductor is the simple *n*-MOSFET source coupled pair shown in figure 1. If we consider that M1 and M2 are in triode region with the same V_{DS}, then I_{D1} and I_{D2} are given by:

$$I_{D1,2} = \beta\left[\left(V_{GS1,2} - V_t\right)V_{DS} - 0.5V_{DS}^2\right], \qquad (1)$$

from which we find:

$$I_{D1} - I_{D2} = \beta V_{DS} v_d \qquad (2)$$

where v_d is the differential input voltage.

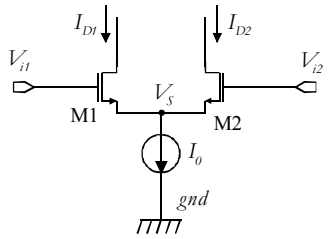

Figure 1: Basic source coupled pair

The transconductance of the stage, G_{m1}, is then given by βV_{DS}, thus tuning can be simply accomplished by varying the V_{DS} of the pair. Now, let us calculate the maximum differential mode voltage. The currents I_{D1} and I_{D2} can be written as:

$$I_{D1,2} = \frac{I_0}{2} \pm \beta V_{DS} \frac{v_d}{2} \qquad (3)$$

Substituting this expression in Eqn. (1), gives the

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following expression for M1 and M2 gate overdrive voltages:

$$V_{GS1,2} - V_t = \frac{I_0}{2\beta V_{DS}} + \frac{V_{DS}}{2} \pm \frac{v_d}{2} \quad (4)$$

Imposing the condition $V_{GS1,2}$-V_t>V_{DS}, to maintain M1 and M2 in triode region, we obtain the maximum v_d value:

$$v_{dmax} = 2(V_{ovd} - V_{DS}) = \frac{I_0}{\beta V_{DS}} - V_{DS} \quad (5)$$

where V_{ovd} is the gate overdrive voltage for v_d=0. In order to obtain a large input differential range (± v_{dmax}), a large gate overdrive voltage is required. Unfortunately, Eqn. (4) indicates that, if the current I_0 is kept constant, the gate overdrive includes a term inversely proportional to V_{DS}. As a consequence, it is not possible (i) to get large V_{ovd} at large V_{DS} and, at the same time, (ii) to prevent V_{ovd} from getting excessively large at small V_{DS}. It is worth mentioning that V_{ovd} affects the minimum input common mode voltage, V_{Cmin}, through the equation:

$$V_{C\min} = V_{GS0} + V_{\min} = V_{ovd} + V_{tn} + V_{\min} \quad (6)$$

where V_{min} is the minimum output voltage of the current source I_0. This problem, that practically would reduce the available tuning range, is mitigated by making I_0 vary as V_{DS}. In the implementation described in next section, we derive V_{DS} and I_0 from the same tuning current I_{tune}, according to the formulas:

$$I_0 = k_1 I_{tune}; \quad V_{DS} = RI_B; \quad I_B = k_2 I_{tune} \quad (7)$$

In this way the gate overdrive voltage becomes:

$$V_{ovd} = V_{ovd}(0) + \frac{V_{DS}}{2} \quad \text{with } V_{ovd}(0) = \frac{k_1}{2\beta k_2 R} \quad (8)$$

where $V_{ovd}(0)$ indicates the V_{ovd} limit for $V_{DS} \to 0$, while v_{dmax} is given by:

$$v_{dmax} = 2V_{ovd}(0) - V_{DS} = \frac{k_1}{\beta k_2 R} - V_{DS} \quad (9)$$

Recalling that G_{m1}=βV_{DS}, we can obtain a very small transconductance by reducing V_{DS} without degradation of either the differential or the common mode input range.

3 TOPOLOGY OF THE PROPOSED TRANSCONDUCTOR

Figure 2 shows the proposed circuit, where M1 and M2 are the input transistors in triode region while the other elements convey I_{D1} and I_{D2} to the output node and impose the same V_{DS} to M1 and M2. Differently from Refs. [2,3] the input common mode range is left free to vary in a wide range. This is obtained by means of a proper feedback loop based on a Three Input Amplifier (TIA) that senses V_{D1}, V_{D2} and V_S, as shown in the figure.

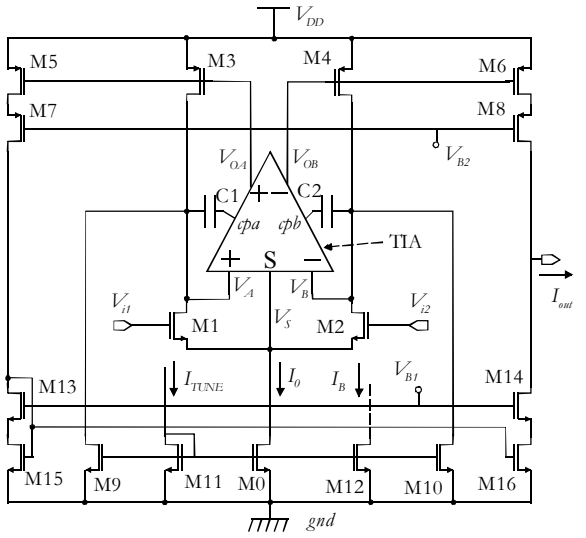

Figure 2: Complete schematic diagram of proposed transconductor. I_B provide biasing of the TIA block; V_{B2} and V_{B2} are bias voltages for the M5-8 and M13-16 cascode mirrors, respectively.

Let us first define the ratios:

$$k_1 = \frac{\beta_0}{\beta_{11}}; \quad k_2 = \frac{\beta_{12}}{\beta_{11}}; \quad (10)$$

The TIA is biased by the current I_B (the connection to the amplifier symbol is not shown for simplicity) and has the following transfer function:

$$V_{OD} \equiv V_{OA} - V_{OB} = A_{dd}(V_A - V_B)$$
$$V_{OC} \equiv \frac{V_{OA} + V_{OB}}{2} = A_{cc}\left(\frac{V_A + V_B}{2} - V_S - RI_B\right) \quad (11)$$

where both A_{dd}>>1 and A_{cc}>>1, while R is a constant resistance value. Note that M3 and M4 form a differential common source output stage cascaded to the TIA, so that the resulting amplifier is closed in negative feedback for both the differential and common mode voltages of inputs V_A and V_B. The common mode voltage is compared to the auxiliary input V_S and amplified with an input offset RI_B. The high gain of both feedback loops assures that the following approximations hold:

$$V_A - V_S = V_B - V_S = RI_B = k_2 RI_{tune} \quad (12)$$

Therefore, the TIA forces V_{DS1} and V_{DS2} to be equal and fixed to a value, tunable by varying I_{tune}. If we add that I_0=$k_1 I_{tune}$ than conditions (7) hold for the M1 and M2 differential pair. Note that no requirement for constant input common mode range of the differential pair has been introduced.

In order to calculate the output current we define the ratios:

$$k_3 = \frac{\beta_5}{\beta_3} = \frac{\beta_6}{\beta_4}; \qquad k_4 = \frac{\beta_9}{\beta_{11}} = \frac{\beta_{10}}{\beta_{11}} \tag{13}$$

Since the cascode mirror M13-16 has unity current gain, we have:

$$I_{out} = k_3\left(I_{D3} - I_{D4}\right) = k_3\left[\left(I_{D2} + I_{D10}\right) - \left(I_{D1} + I_{D9}\right)\right] \tag{14}$$

Finally, considering that nominally $I_{D10}=I_{D9}=k_4 I_{tune}$, and applying Eq. (2) and (7) we get:

$$I_{out} = G_m v_d \quad \text{with} \quad G_m = k_3 k_2 \beta R I_{tune} \tag{15}$$

Currents I_{D9} and I_{D10}, being nominally equal by design, do not affect the output current. They prevent M3 and M4 from being turned off when a large differential signal completely unbalance the input transistors. In practice, we guarantee that $I_{D3}, I_{D4} \geq k_4 I_{tune}$, with the benefit of avoiding excessive phase margin degradation deriving from the reduction of M3 and M4 pole/zero frequencies. In addition, every bias current is made proportional to I_{tune}, in order to let all the circuit singularities vary coherently over the whole tuning range, thus stabilizing the phase margin of the loops.

The complete TIA schematic is shown in figure 3, with numbers placed close to transistors forming current mirrors to indicate the related current gains.

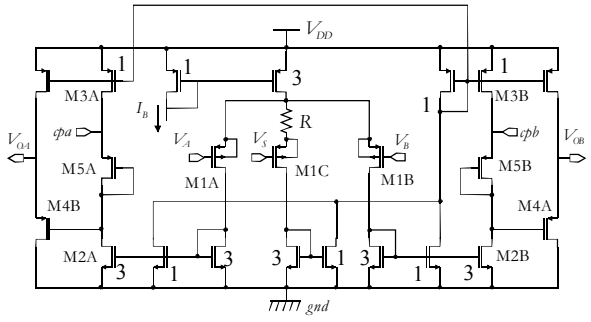

Figure 3: TIA complete schematic diagram.

The differential output stages are formed by M2A,M3A and M2B,M3B. The role of diode connected transistors M5A and M5B will be shown later. M4A and M4B form level shifter to provide correct driving to transistors M4-M3 of the global transconductor (figure 2). From simple inspection of the circuit, we found that

$$I_{D3A} = I_{D3B} = \left(I_{D1A} + I_{D1C} + I_{D1B}\right)/3 = I_B \tag{16}$$

Therefore I_{D3A} and I_{D3B} do not depend on the input signals. On the other hand, $I_{D2B}=I_{D1B}$ and $I_{D2A}=I_{D1A}$. It can be easily shown that, considering infinite MOSFET output resistances, the output ports are non saturated only if $I_{DA1}=I_{DB1}=I_{DC1}=I_B$. Since M1A, M1B and M1C are identical, they have identical V_{GS}, hence Eqns. (12) are proven. From this quiescent conditions, if we apply a common mode signal to V_A and V_B, I_{D2A} and I_{D2B} vary of the same amount and so do the outputs. Instead, an input differential mode varies I_{D2B} and I_{D2A} of opposite quantities, producing only a differential mode on the outputs. This provides an heuristic justification of Eqns. (11). Compensation of the frequency response is attained by a Miller scheme, made possible by the two-stage nature of the TIA and M3-M4 cascade. The role of zero nulling resistors (of value $1/g_m$) is played by M5A and M5B. To understand this, consider that M3A and M3B are open circuit in the small signal equivalent circuit. M5A and M5B are biased with a current proportional to I_{tune}, in order to track the g_m of M3-M4, maintaining a sufficient phase margin of the loops over the whole tuning range.

As far as input referred voltage noise and offset are concerned, the large current division operated by the output mirrors (k_3), emphasizes the contribution of the output transistors M5,M6,M15,M16. The TIA offset and noise unbalance the V_{DS} of the input transistors, giving a larger contribution at the lowest end of the tuning range, where V_{DS} is smaller. A quantitative analysis on this aspect is beyond the aim of this paper.

4 SIMULATED PERFORMANCES

A transconductor, optimized for a 0.5-5 nS G_m range, has been designed using the Bipolar-CMOS-DMOS BCD6 process of STMicroelectronics, using only devices from the 0.35 µm-3.3 V CMOS subset. The most relevant data are the following: k_1=1, k_2=30, k_3=0.02, k_4=2, $W_{1,2}$=1 µm, $L_{1,2}$=200 µm, $L_{5\text{-}8}$=170, $W_{13\text{-}16}=W_{5\text{-}8}$=1.5, $L_{13\text{-}16}$=200, R=50 kΩ, $C_1=C_2$=10 pF. The circuit was characterized by means of DC simulations, using the electric simulator ELDO™, with Philips 9 device models provided by STMicroelectronics. For all the configurations analyzed, transient simulations were used to prove the circuit stability. All the following tests were performed with V_{dd}=3.3 V, and the output terminal shorted to a $V_{dd}/2$ ideal voltage source. Figure 4 shows the G_m behaviour as a function of v_d, for various values of the tuning current. In agreement with Eqn. (9), the region where the G_m can be considered constant, progressively decreases as I_{tune} (i.e. V_{DS}) is increased. Residual G_m variation with v_d visible in the constant-G_m regions can be ascribed to phenomena not represented in Eqn.(1), such as vertical field induced mobility degradation.

A tuning ratio of about 1:10 can be observed for tuning currents varying from 30 to 300 nA. In this interval, all the transistors are biased in strong inversion region.

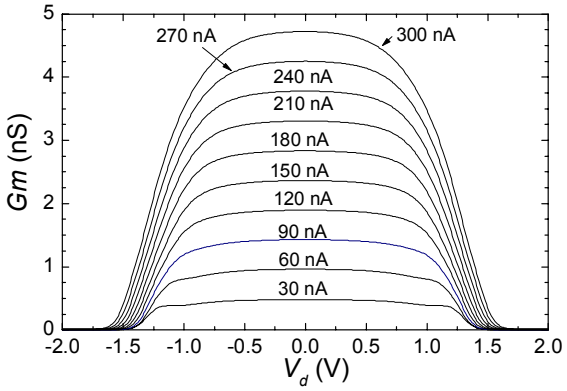

Figure 4: G_m vs. v_d for various tuning currents.

The tuning law (G_m vs. I_{tune}) is shown in figure 5 for three temperatures. The curves provide a qualitative confirmation of Eqn. (15). In particular, the curves are linear with a slope that decreases when the temperature increases, as could be reasonably expected from the presence of the electron mobility factor in the G_m expression.

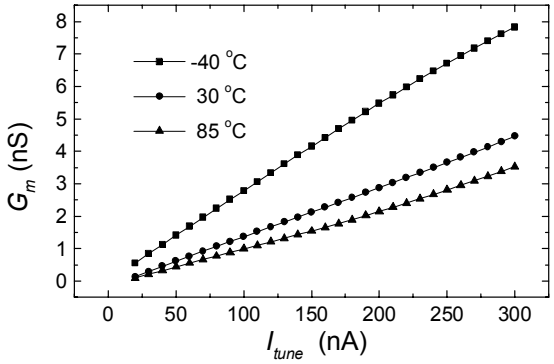

Figure 5: Tuning law for three different temperatures.

The plots shown in figure 4 and 5 have been obtained with an input common mode voltage (V_{cm}) of 2 V. The fact that an interval exists, where V_{cm} can be freely varied without perturbing the transconductor correct operation, is partially confirmed by figure 6.

We observe that the overall transconductance G_m actually presents only a weak dependence on V_{cm} when the latter varies approximately from 1.9 V to V_{dd}. In this range, the relative variation is less than 9 % for all the curves shown. The slight G_m decrease visible in the figure, can again be ascribed to the low accuracy of Eqn.(1). Below the interval of nearly-constant G_m, large variations occur. Considering the large overdrive voltage chosen for M1,2 (0.6-0.8 V) in order to maximize the differential input range, this limit can be expected from Eqn.(6).

Note that Eqns. (5) and (6) indicate that a trade-off between differential and common mode range should be managed during the design phase, depending on the application.

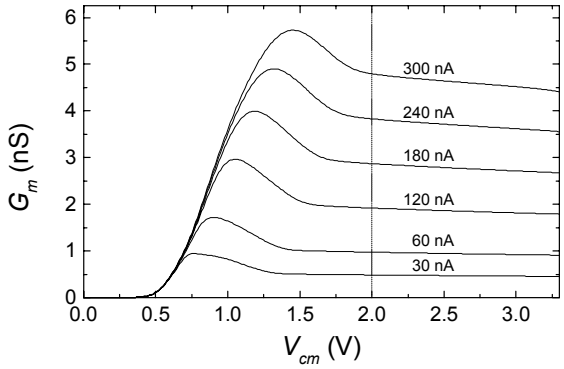

Figure 6: G_m plots as a function of the input common mode voltage for various tuning current values.

5 CONCLUSIONS

The simulated results confirm the prediction of a G_m linearly dependent on the tuning current, with a maximum input differential range available at the smallest G_m values. This facilitates the design of ultra-low frequency fully integrated filters. The circuit performances are maintained when the input common mode is varied over a wide interval. The problem of the large sensitivity to temperature can be overcome using DC master-slave architectures [4].

Acknowledgments

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