CMOS Transconductors With Nearly Constant Input Ranges Over Wide Tuning Intervals

Paolo Bruschi, Fabio Sebastiano, and Nicolò Nizza

***Abstract*—Three different bias strategies aimed to reduce the effect of tuning on either the differential input range or the common-mode range of triode-region CMOS transconductors are presented. The method is applied to an original transconductor topology that is optimized to produce ultralow G_m values. A prototype circuit, which was designed with the 0.35-μm bipolar-CMOS-DMOS (BCD6) process of STMicroelectronics, is presented. The effectiveness and limitations of the method are characterized by means of electrical simulations.**

***Index Terms*—CMOS transconductor, constant input range, low-frequency filters.**

I. Introduction

In G_m–C filters, the transconductor input common-mode range (CMR) and differential-mode range (DMR) have different impacts on the maximum signal amplitude, depending on the particular filter architecture. The CMR plays an important role in single/ended filters, especially for the in-band performances of low-pass filters [1]. On the other hand, a wide DMR is essential in high-Q filters, either in single/ended or fully differential configurations [2], [3]. Unfortunately, CMOS transconductors generally present input ranges that are strongly dependent on tuning. In transconductors using either saturated active elements or transistors in linear region as tunable resistors, both G_m and the DMR are proportional [4] to the overdrive voltage $V_{\rm GS} - V_t$. For this reason, the DMR is minimum at the lowest end of the tuning interval. Conversely, using active elements in the triode region, the DMR is still tied to the overdrive voltage, while the G_m is proportional to $V_{\rm DS}$.

In this brief, we present three different bias strategies that exploit this additional degree of freedom to obtain constant DMR, constant CMR, and a tradeoff situation, respectively. To our knowledge, biasing methods aimed to obtain constant input ranges over large tuning intervals have not been presented in the literature.

The methods have been applied to a recently proposed transconductor [5], which is briefly described in Section II. The biasing strategies and circuits are detailed in Section III, and their effectiveness and limits are illustrated by electrical simulations in Section IV. The transconductor is optimized for producing ultrasmall G_ms for application in single/ended low-frequency filters. It should be observed that although the most intriguing results in the field of G_m–C filters comes from high-frequency applications, the growing interest in integrated mechanical, chemical, and thermal sensors urged the development of fully integrated filters with singularities of the order of hundreds of hertz or below [6]–[8]. Using the on-chip capacitors available in standard microelectronic processes, G_m's in the range of a few nanosiemens or below are required. In this respect, the choice of using transconductors with active elements in the triode region gives an additional advantage, deriving from the mentioned G_m proportionality to $V_{\rm DS}$. Differently from the overdrive voltage, the $V_{\rm DS}$ can be reduced with no risk of getting out of the strong inversion region. Since the $V_{\rm DS}$ lower limit is practically due to noise only, very low G_m values can be in principle obtained with moderate transistor size and current division factors.

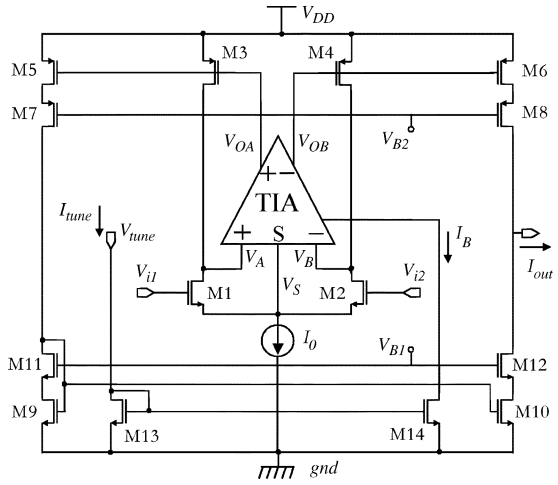

Fig. 1. Transconductor simplified schematic view.

II. Transconductor Topology and Operating Principle

The transconductor simplified schematics is shown in Fig. 1.

Additional components that were used to guarantee stability and were not essential to understand the dc operation, as well as the subcircuit producing the voltages $V_{\rm B1}$ and $V_{\rm B2}$, which bias the cascode mirrors M5–M8 and M9–M12, have been omitted in this description. More details about transconductor stability can be found in [5]. As will be shown later, the three-input amplifier (TIA) sets the values of the M1 and M2 drain–source voltages $V_{\rm DS}$. Supposing that M1 and M2 are in the triode region, using the usual square law expression, we have

$$I_{\rm D1,2} = \beta\left[\left(V_{\rm GS1,2} - V_t\right)V_{\rm DS} - 0.5V_{\rm DS}^2\right] \qquad (1)$$

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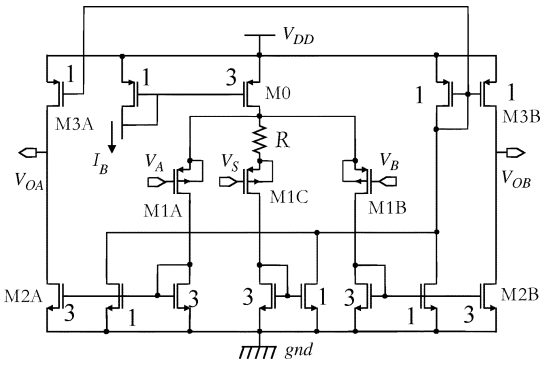

Fig. 2. Simplified schematic of the TIA. Current mirror gains are indicated by numbers close to the MOSFETs involved.

where $\beta = \mu_n C_{\rm ox} W_1/L_1$, μ_n is the electron effective mobility, $C_{\rm ox}$ is the gate capacitance per unit area, and W_1/L_1 indicates the M1 and M2 aspect ratio. The drain current difference is then

$$I_{\rm D1} - I_{\rm D2} = \beta V_{\rm DS} v_d \tag{2}$$

where v_d is the input differential voltage $V_{\rm i1} - V_{\rm i2}$.

The TIA simplified schematic is shown in Fig. 2, where R is a constant resistor. The circuit is symmetrical, and M1C is equal to M1A and M1B.

To understand how the TIA works, let us write the outputs $V_{\rm OA}$ and $V_{\rm OB}$ as a superimposition of a quiescent voltage V_M and a linear contribution, which were calculated using the Norton equivalent circuit of the output ports given by

$$\begin{aligned} V_{\rm OA} &= V_M + r_{\rm out}(I_{\rm D3A} - I_{\rm D2A}) = V_M + r_{\rm out}(I_B - I_{\rm D1A}) \\ V_{\rm OB} &= V_M + r_{\rm out}(I_{\rm D3B} - I_{\rm D2B}) = V_M + r_{\rm out}(I_B - I_{\rm D1B}) \end{aligned} \tag{3}$$

where $r_{\rm out}$ is the output resistance, which is given by

$$r_{\rm out} = r_{\rm d2A} || r_{\rm d3A} = r_{\rm d2B} || r_{\rm d3B}. \tag{4}$$

Considering all the mirrors as ideal, V_M is the output voltage when $I_{\rm D1A} = I_{\rm D1B} = I_{\rm D1C}$, i.e., $V_{\rm GS1A} = V_{\rm GS1B} = V_{\rm GS1C}$, which is obtained for the particular input condition

$$V_A - V_S = V_B - V_S = RI_B. \tag{5}$$

First-order approximation around this point gives

$$I_{\rm D1A,B} = I_B \pm \frac{g_{\rm md}}{2}(V_A - V_B) + g_{\rm mc}\left(\frac{V_A + V_B}{2} - V_S - RI_B\right) \tag{6}$$

where

$$g_{\rm md} = g_{\rm ma,b,c}, \quad g_{\rm mc} = \frac{g_{\rm md}}{3 + 2g_{\rm md}R}. \tag{7}$$

Substituting (6) into (3), we obtain

$$\begin{aligned} V_{\rm OD} &\equiv V_{\rm OA} - V_{\rm OB} = A_{\rm dd}(V_A - V_B) \\ V_{\rm OC} &\equiv \frac{V_{\rm OA} + V_{\rm OB}}{2} \\ &= A_{\rm cc}\left(\frac{V_A + V_B}{2} - V_S - RI_B\right) + V_M \end{aligned} \tag{8}$$

where $A_{\rm dd} = g_{\rm md} r_{\rm out}$ and $A_{\rm cc} = g_{\rm mc} r_{\rm out}$ are factors that can be easily sized to be both much larger than one.

In Fig. 1, the cascade of the TIA and the M3–M4 common source differential stage forms a fully differential amplifier, with both the differential- and common-mode gains much larger than 1. Furthermore, (8) indicates that an offset term RI_B is present in the common-mode transfer function, when V_S is used as a reference terminal for V_A and V_B. In Fig. 1, the input and the output ports of this amplifier are connected together to form a negative feedback loop with both the common-mode and differential-mode loop gains much higher than 1. It can be easily shown that in this condition, the larger the loop gains, the closer the input voltages V_A and V_B satisfy (5). Thus, due to the way the TIA inputs are connected to the M1 and M2 terminals and the reasonably high gains of the TIA-M3-4 cascade, the required condition $V_{\rm DS1} = V_{\rm DS2} = RI_B$ is satisfied with good approximation.

Defining the following ratios:

$$k_{\rm out} = \frac{\beta_5}{\beta_3} = \frac{\beta_6}{\beta_4}, \quad k_{\rm tune} = \frac{\beta_{14}}{\beta_{13}} \tag{9}$$

and considering that the current ratio of mirror M9–12 is one, we finally obtain the overall G_m of the cell

$$G_m = I_{\rm out}/v_D = \beta k_{\rm out} k_{\rm tune} R I_{\rm tune}. \tag{10}$$

III. Optimization of the Input Ranges

Using (1) and (2), we can easily derive the following expressions for the M1 and M2 gate overdrives:

$$V_{\rm GS1,2} - V_t = \frac{I_0}{2\beta V_{\rm DS}} + \frac{V_{\rm DS}}{2} \pm \frac{v_d}{2}. \tag{11}$$

The maximum input differential voltage is determined by the requirement for M1 and M2 to remain in the triode region. Imposing $V_{\rm GS} - V_{\rm tn} > V_{\rm DS}$ in (11), we obtain

$$\max(v_d) = 2\left(\frac{I_0}{2\beta V_{\rm DS}} - \frac{V_{\rm DS}}{2}\right). \tag{12}$$

As far as the CMR is concerned, it can be proven that the upper limit occurs when transistor M0 of the TIA goes into the triode region. Considering both Figs. 1 and 2, we find that the maximum input common mode $\max(V_C)$ is given by

$$\max(V_C) = V_{\rm DD} - |V_{\rm GS0} - V_{\rm tp}| - |V_{\rm GS1A}| + V_{\rm GS} - V_{\rm DS} \tag{13}$$

where $V_{\rm tp}$ is the p-MOSFET threshold voltage, while $V_{\rm GS}$ and $V_{\rm DS}$ are related to the input transistors M1 and M2. Equation (13) can be rewritten as

$$\begin{aligned} \max(V_C) = V_{\rm DD} - |V_{\rm GS0} - V_{\rm tp}| - |V_{\rm GS1A} - V_{\rm tp}| \\ + V_{\rm ov} - V_{\rm DS} + (V_{\rm tn} - |V_{\rm tp}|) \end{aligned} \tag{14}$$

where $V_{\rm tn}$ is the threshold voltage of M1 and M2, while $V_{\rm ov}$ is the gate overdrive for null input differential voltage, which is given by (11) with $v_d = 0$.

Note that $(V_{\rm ov} - V_{\rm DS})$ should be positive in order to keep M1 and M2 in the triode region. Furthermore, $V_{\rm tn}$ is likely to be greater than $|V_{\rm tp}|$ since due to the bulk connection of M1A and M1B, the latter one is not affected by the body effect. As a consequence, the upper limit of the CMR is close to $V_{\rm DD}$ or even gets higher than $V_{\rm DD}$ in the case of large $V_{\rm ov}$. Therefore,

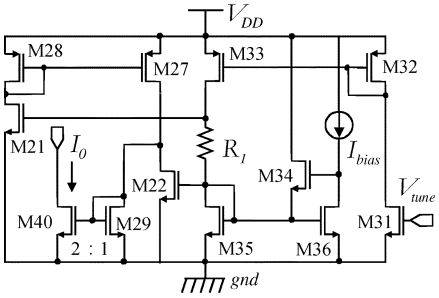

Fig. 3. Circuit used to produce I_0 for the case of $\delta = 1$.

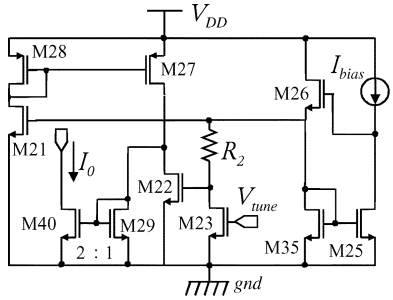

Fig. 4. Circuit used to produce I_0 for the case of $\delta = -1$.

the CMR upper limit is not of concern and will be neglected in the rest of this brief. Thus, the CMR will be constrained mainly by its lower limit, which is given by

$$\min(V_C) = V_{\min} + V_{\rm ov} + V_{\rm tn} \tag{15}$$

where $V_{\min}$ is the minimum output voltage of the current source I_0.

So far, we have considered I_0 as a constant. If this were the case, then $V_{\rm DS}$ variations, which were applied to tune the G_m, would strongly modify both the differential input range and the gate overdrive $V_{\rm ov}$, which in turn affects the CMR through (15). To limit this effect, I_0 is made to vary with $V_{\rm DS}$ according to the formula

$$I_0 = g_0 V_{\rm DS} + \delta\beta V_{\rm DS}^2 \tag{16}$$

where g_o is a constant conductance and δ can assume the values

$$\delta = \{0, 1, -1\}. \tag{17}$$

Substituting the expression of I_0 into (11) and (12), gives

$$V_{\rm ov} = \frac{g_0}{2\beta} + \frac{V_{\rm DS}}{2}(1+\delta)$$
$$\max(v_d) = 2\left[\frac{g_0}{2\beta} - \frac{V_{\rm DS}}{2}(1-\delta)\right]. \tag{18}$$

It can be easily observed that a constant DMR over the whole tuning range can be obtained with $\delta = 1$. On the contrary, with $\delta = -1$, the input transistor gate overdrive $V_{\rm ov}$ does not depend on tuning, as well as the lower limit of the input common-mode voltage, provided that the dependence of $V_{\min}$ on I_0 can be neglected. An intermediate situation with moderate effects of $V_{\rm DS}$ on both the DMR and CMR is obtained for $\delta = 0$.

The circuit used to produce a current I_0 that varies according to (16) with $\delta = 1$ is shown in Fig. 3. All the current mirrors present in the circuit have gains equal to 1, except for the mirror M40–M29, whose gain is 2. Thus, the current I_0 is equal to twice the difference $I_{\rm D21} - I_{\rm D22}$.

M34–M36 form a Wilson mirror that fixes the drain current in M35 to the constant current $I_{\rm bias}$. Therefore, the M22 gate–source voltage, which is indicated with V_0, is constant and equal to

$$V_0 = V_{\rm tn} + \sqrt{\frac{2I_{\rm bias}}{\beta_{35}}} \tag{19}$$

where $\beta_{35} = \beta_n C_{\rm ox} W_{35}/L_{35}$. The gate of M31 is connected to the node $V_{\rm tune}$ in Fig. 1 so that $I_{\rm D31}$ is proportional to the TIA bias current I_B, which in turn is proportional to $V_{\rm DS}$, as stated in the previous section. The current $I_{\rm D31}$ is mirrored into R_1 by M32–M33. With a proper choice of R_1 and of the M31 aspect ratio, the voltage drop across R_1 is made equal to $V_{\rm DS}$. Thus, the M21 gate–source voltage is given by $V_0 + V_{\rm DS}$.

Finally, M21 and M22 are replicas of the transconductor input transistors M1 and M2. With the preceding assumptions, I_0 is given by

$$I_0 = 2\left[\frac{\beta}{2}(V_0 - V_{\rm tn} + V_{\rm DS})^2 - \frac{\beta}{2}(V_0 - V_{\rm tn})^2\right]. \tag{20}$$

It is easy to verify that (20) is equivalent to (16), where $\delta = 1$ and

$$g_0 = 2\beta(V_0 - V_{\rm tn}). \tag{21}$$

A similar circuit, which is shown in Fig. 4, is used to produce a current I_0 that follows (13) with $\delta = -1$. Again, M23 makes a replica of I_B flowing through R_2 in order to produce a voltage drop equal to $V_{\rm DS}$ across the resistor itself. The current I_0 is still given by $2(I_{\rm D21} - I_{\rm D22})$, but now $V_{\rm GS21}$ is to be fixed to the value indicated in (19). Therefore, $V_{\rm GS22}$ is equal to $V_0 - V_{\rm DS}$, and with simple passages, the correct operation of the circuit can be demonstrated.

The third case, i.e., $\delta = 0$, requires that I_0 is proportional to $V_{\rm DS}$ and consequently, to $I_{\rm tune}$. Thus, to produce I_0 for $\delta = 0$, it is simply necessary to mirror the current $I_{\rm tune}$ with a proper gain k_0 so that from (5), (9), and (16), g_o is given by

$$g_0 = \frac{k_0}{R \cdot k_{\rm tune}}. \tag{22}$$

It should be observed that g_o is an important parameter that appears in both the DMR and CMR through (18). In particular, g_o fixes the quiescent gate overdrive of the input transistors. A large $V_{\rm ov}$ results in large DMR and reduced CMR and vice versa.

IV. Simulated Results and Discussion

The effectiveness of the proposed circuits has been demonstrated by means of simulations performed on a prototype designed with the 0.35-μm 3.3-V CMOS devices of the bipolar-CMOS–DMOS process BCD6 provided by STMicroelectronics. The test transconductor was sized to produce G_m

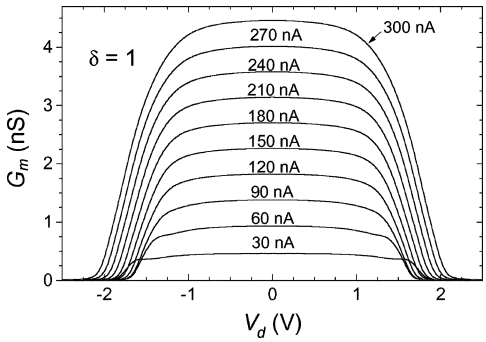

Fig. 5. G_m as a function of the input differential voltage for various tuning currents in the case of $\delta = 1$. The common-mode voltage is fixed at 2.1 V.

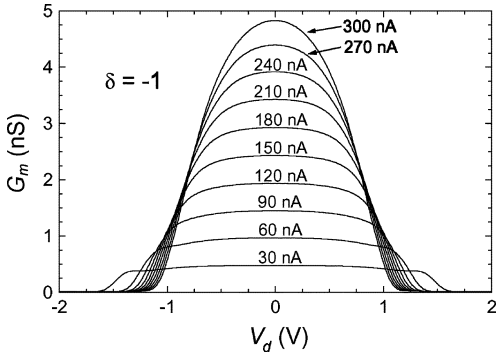

Fig. 6. G_m as a function of the input differential voltage for various tuning currents in the case of $\delta = -1$. The common-mode voltage is fixed at 2.1 V.

values in the range of nanosiemens, which are intended for application to very low frequency filters. The main data about the implementation are the following: $k_{\rm tune} = 30$, $k_{\rm out} = 0.02$, $W_{1,2} = 1\ \mu$m, $L_{1,2} = 200\ \mu$m, $R = R_1 = R_2 = 50$ kΩ, and $V_{\rm dd} = 3.3$ V. The tuning current $I_{\rm tune}$ was varied between 30 and 300 nA, resulting in $V_{\rm DS}$ variation in the range of 45–450 mV.

In order to compare the three biasing strategies that correspond to the conditions $\delta = 0$, 1, -1, we individually adjusted g_0 in the three cases to have approximately the same I_0 value at the lowest end of the tuning range. In practice, we fixed $I_0 = I_{\rm tune}$ for the case of $\delta = 0$ by simply setting $k_0 = 1$ in (22). Then, we individually adjusted the circuits of Figs. 3 and 4, which were used for the cases of $\delta = 1$ and $\delta = -1$, by setting a V_0 value, resulting in $I_0 \approx 30$ nA for $I_{\rm tune} = 30$ nA, as for $\delta = 0$. The gate overdrive $V_{\rm ov}$ was then about 0.65 V at the lowest end of the tuning range for all the three bias methods. Due to the different dependence of I_0 on $I_{\rm tune}$, different $V_{\rm ov}$ values and input ranges are explored by increasing $I_{\rm tune}$ along the tuning range.

Fig. 5 shows G_m as a function of the input differential voltage in various tuning conditions for the case of $\delta = 1$. According to (18), the zone of nearly constant G_m is not significantly affected by tuning. Residual G_m variation in the flat area can be ascribed to phenomena not modeled by (1), such as vertical-field-induced mobility degradation [9].

The linearity of the tuning law predicted by (10) is also confirmed by the even spacing of the curves. Note that (10) does not depend on the current I_0; therefore, a linear G_m versus $I_{\rm tune}$ behavior should be expected also for the other biasing strategies. Fig. 6, which shows the G_m versus v_d curves for the case of $\delta = -1$, confirms this prediction and at the same time, shows a progressive reduction of the DMR as the tuning current is increased. Since $V_{\rm DS}$ is proportional to $I_{\rm tune}$, the results of Fig. 6 are in agreement with (18).

An intermediate situation [5] with DMR decreasing to a lower rate than in Fig. 6 is obtained for $\delta = 0$.

The $\pm$3-dB transconductance upper frequency limit was around 8 kHz at the minimum G_m value (0.48 nS) regardless of the biasing strategy and shifts to 20 kHz at the maximum G_m value (4.8 nS).

The CMR was estimated by plotting the overall G_m as a function of the input common-mode voltage, with $v_d = 0$. The result

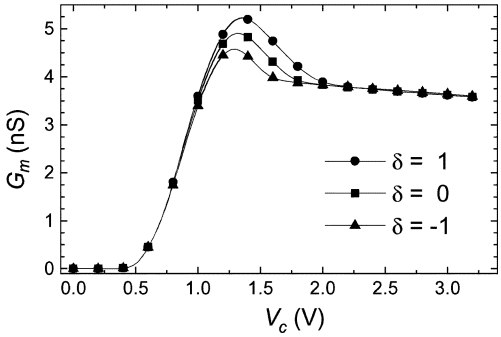

Fig. 7. Plot of G_m as a function of the input common-mode voltage V_c for the three different biasing options $\delta = 1$,0,-1. The curves have been simulated with $v_d = 0$ and $I_{\rm tune}$ close to the upper limit.

for the three biasing strategies and the transconductor tuned to produce a G_m of about 3.8 nS is shown in Fig. 7. Note that G_m presents a moderate dependence on the input common-mode voltage in an interval extending from a given lower limit $V_{\rm cmin}$ to $V_{\rm DD}$. Below this interval, large G_m variations can be observed.

The fact that G_m is not strictly constant for $V_C > V_{\rm cmin}$ is partly due to the finite output resistance of M0 (see Fig. 2) causing the TIA bias current to depend on the common-mode voltage. The three curves in Fig. 7 have not been obtained with the same $I_{\rm tune}$ value, but small adjustments were required to make the curves coincide in the flat region.

As predicted in Section III, the CMR stretches up to $V_{\rm DD}$ in all conditions, while its lower limit depends on the biasing method. Note that the curves tend to coincide when the transconductor is tuned for the minimum G_m since for the sizing previously described, the current I_0 becomes the same in the three cases.

In order to provide a more quantitative comparison of the biasing method, the effective width of the DMR and CMR has been estimated from simulations similar to those shown in Figs. 5–7. In particular, the DMR was set equal to $\max(v_d)$, which is defined as the v_d value at which the G_m drops below 10% of the value for $v_d = 0$. This corresponded to a total harmonic distortion (THD) that varies from 0.6% to 0.8% and is estimated by means of transient simulations with sinusoidal input signals of frequency in the range of 1–100 Hz. The CMR was defined as $V_{\rm DD} - V_{\rm cmin}$, where $V_{\rm cmin}$ was chosen in such

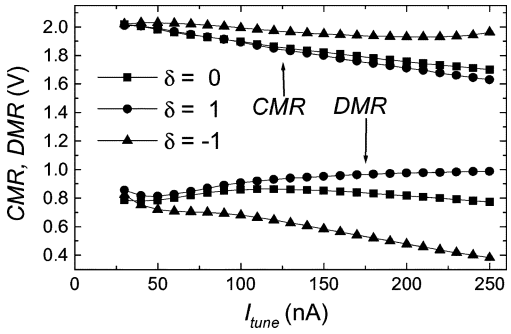

Fig. 8. CMR and DMR as a function of the bias current for the three biasing options. The DMR is $\max(v_d)$, while the CMR is $V_{\rm DD} - V_{\rm cmin}$.

a way that the total G_m variation over the interval $[V_{\rm cmin}, V_{\rm DD}]$ is $\pm 10\%$ of the value taken in the middle of the interval itself. The results for both the DMR and CMR are shown in Fig. 8.

As predicted by (12) and (15), there is clear evidence that the case of $\delta = -1$ produces the best CMR stabilization. As far as the DMR stabilization is concerned, optimum performance is expected for $\delta = 1$. Fig. 8 shows that the bias option $\delta = 1$ actually results in the flattest curve at higher $I_{\rm tune}$ values, although the performance in terms of overall variation is similar to the case of $\delta = 0$.

Monte Carlo simulation showed that process variations and component mismatch affect the width of the DMR and CMR ($\pm 10\%$ maximum variation) but not the way they vary with tuning, according to the selected bias strategy. A large input offset voltage (± 75 mV at 3σ) was observed.

V. Conclusion

Combination of the proposed transconductor topology with the three biasing methods resulted in three distinct cells, all marked by moderate input voltage range variations along the whole tuning curve. The DMR or alternatively the CMR can be effectively kept constant by selecting the particular method that corresponds to $\delta = 1$ or $\delta = -1$, respectively. The option $\delta = 0$, which is implemented using a much simpler circuit, provides a tradeoff, which turned out to be more similar to the case of $\delta = 1$ rather than $\delta = -1$.

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